CLAIMS

What is claimed is:

1. A driver set for a cross point memory array comprising:

a semiconductor substrate;

a plurality of line driver groups formed on the substrate, each line driver group having N line drivers;

a plurality of contiguous conductive lines, each conductive line electrically connected to both a line driver and a row of memory cells, each memory cell being fabricated to a width W;

wherein the line driver group has a width that is not greater than N x W.

2. The driver set of claim 1, wherein:

the plurality of conductive lines connect to a plurality of rows of memory cells such that the line driver groups are no wider than the plurality of rows of memory cells.

3. The driver set of claim 1, wherein:

W is equal to the pitch of a conductive line, whereby the pitch is the minimum feature size added to the minimum spacing between features.

4. The driver set of claim 3, wherein:

each row of memory cells is situated above the line driver that it is electrically connected to.

5. The driver set of claim 4, further comprising:

no more than 2 levels of metallic interconnect between the line driver and the row of memory cells.

6. The driver set of claim 3, wherein:

the plurality of conductive lines go in either a first direction or a second direction orthogonal to the first direction such that the conductive lines terminate at one of four line edges; and

the line drivers are distributed over the four line edges.

7. The driver set of claim 1, wherein:

N is equal to 8.

8. The driver set of claim 1, wherein:

the width of the driver group is sufficient to contain at least one transistor, whereby any additional transistors that cannot be contained within the width are stacked lengthwise and do not contribute to the width of the driver group.

9. The driver set of claim 8, wherein:

the width of the driver group is sufficient to contain at least a pair of transistors.

10. The driver set of claim 9, wherein:

pairs of transistors share a common node.

11. The driver set of claim 10, wherein:

transistors that share a common node are electrically connected to separate conductive lines.

12. The driver set of claim 11, wherein:

the common nodes of some transistor pairs in the driver group are electrically connected to other peripheral circuitry; and

the common nodes of the remaining transistor pairs in the driver group are electrically connected to a reference voltage.

13. The driver set of claim 12, wherein:

the other peripheral circuitry is a primary decoder, whereby the primary decoder is responsible for selecting a driver group.

14. The driver set of claim 12, wherein:

the reference voltage is ground.

15. The driver set of claim 11, wherein:

three transistor pairs constitute two line drivers in a line driver group.

16. Circuitry for a cross point memory array comprising:

a plurality of line driver groups that are stacked in a first direction, each line driver group having *N* line drivers that control *N* contiguous lines, each line driver being in one of *N* positions;

a primary decoder that is electrically connected to the plurality of line driver groups and is capable of selecting a single line driver group from the plurality of line driver groups;

a secondary decoder that is electrically connected to the plurality of line driver groups and is capable of selecting all the line drivers that are in a selected position from among the *N* positions; and

a memory array that is electrically connected to the plurality of line driver groups via the *N* contiguous lines in each line driver group;

wherein the size of the plurality of line driver groups in the first direction is less than or substantially the same as the size of the memory array in the first direction.

17. The circuitry of claim 16, wherein:

the circuit is used in re-writable memory.

18. The circuitry of claim 16, wherein:

the memory array has memory plugs that exhibit a non-linear resistive characteristic.

19. The circuitry of claim 18, wherein:

the resistive memory elements are formed from conductive metal oxides.

20. The circuitry of claim 16, further comprising:

a second plurality of line driver groups that are stacked in a first direction, each line driver group having N line drivers, each line driver being in one of N positions;

a second primary decoder that is electrically connected to the second plurality of line driver groups and is capable of selecting a single line driver group from the second plurality of line driver groups; and

a second secondary decoder that is electrically connected to the second plurality of line driver groups and is capable of selecting all the line drivers of the second plurality of line driver groups that are in a selected position from the N positions;

wherein the memory array is electrically connected to the second plurality of line driver groups; and

wherein the size of the memory array in the first direction is substantially the same as or greater than the sum of the size of the plurality of line driver groups in the first direction and the size of the second plurality of line driver groups in the first direction.

21. The circuitry of claim 16, further comprising:

an orthogonal plurality of line driver groups that are stacked in a second direction that is orthogonal to the first direction, each line driver group having *M* line drivers, each line driver being in one of *M* positions;

an orthogonal primary decoder that is electrically connected to the orthogonal plurality of line driver groups and is capable of selecting a single line driver group from the orthogonal plurality of line driver groups; and

an orthogonal secondary decoder that is electrically connected to the orthogonal plurality of line driver groups and is capable of selecting all the line drivers of the orthogonal plurality of line driver groups that are in a selected position from the *M* positions;

wherein the size of the memory array in the second direction is substantially the same as or greater than the size of the orthogonal plurality of line driver groups in the first direction.